SUB.: TEST PROCEDURE FOR LP-1 LOGIC PROBE

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1. APPLYING POWER TO THE PROBE :
   The LP-1 is protected against over-Voltage and reverse Voltage on its power leads. Connect the Back Clip Lead to the common (-) and the Red Clip Lead to plus (+) Vcc. In order to minimize the possibility of power supply spikes, or other spurious signals from affecting the operation of the probe, connect the power leads as close to the node to be tested as possible.

2. SETTING THE SWITCHES :
   LOGIC FAMILY DTL / TTL, CMOS :
   Setting the Logic Family switch to the DTL / TTL position programs the LP-1's window comparator for LOGIC "1" or 2.25 Volts □ñ□0.15 Volts and a LOGIC "0" of 0.8 Volts 0.10 Volts. In the CMOS position, LOGIC "1" and LOGIC "0" levels are determined by the applied Vcc. LOGIC "1" > 70% Vcc and LOGIC "0" <30% Vcc. HTL operating at 15 Volts have LOGIC "1" and LOGIC "0" thresholds specified at > 8.5 V and <6.5 Volts. They compare favorably to the 70/30% programming of the LP-1 in the CMOS mode. LOGIC "0" levels can be user defined by using a power source external to the circuit supply.

3. LOGIC LEVEL TEST :
   TEST EQUIPMENT NEEDED :
   5V DC Regulated Power Supply.
   3-digit DVM, 1 Meg□ê□ Input.
   1K Linear Potentiometer.

   LOGIC LEVEL TEST CIRCUIT
   DTL / TTL TEST :

1. DTL / TTL - CMOS Switch in the DTL / TTL Position.
2. PULSE / MEM Switch in the Pulse Position.
3. Adjust the 1K Potentiometer until the Low LED goes on. Max. Logic "0" Voltage 0.9 Volts. Min. Logic "0" Voltage 0.7 Volts.
4. Adjust the 1K Potentiometer until the HI LED goes on.
   Max. Logic "1" Voltage 2.55 Volts.
   Min. Logic "1" Voltage 2.10 Volts.

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CMOS TEST :

1. DTL / TTL - CMOS Switch in the CMOS Position.
2. PULSE / MEM Switch in the Pulse Position.
3. Adjust the 1K Potentiometer until the LO LED lights Max. Ligic "0" Voltage 1.7 Volts. Min. Logic "0" Voltage 1.35 Volts.
4. Adjust the 1K Potentiometer until the HI LED lights.
   Max. Logic "1" Voltage 3.85 Volts. Min. Logic "1" Voltage 3.15 Volts.
   The test CMOS Logic Levels above 5 Volt Vcc Refer to CMOS/Vcc Graph on Page 5. Logic Level should be within □ñ□10% of curves.

4. PULSE TEST :

   TEST EQUIPMENT NEEDED :

   5V DC Regulated Power Supply.
   Pulse Generator output 600 of less (CSC Model 4001 or equivalent).
   Oscilloscoe, input 1 Meg□ê□ or more.
   Shunt Capacitor, 100pF or less.

   PULSE TEST CIRCUIT

   DTL / TTL TEST :

1. DTL / TTL - CMOS Switch in the DTL / TTL Position.
2. PULSE / MEM Switch in the Pulse Position.
3. Pulse Generator set to :
4. Pulse LED will flash.

MEMORY TEST :

1. PULSE / MEM Switch in the MEM Position.
2. Test in the Pulse Test Circuit.
3. Pulse LED will stay on.

NOTE : The Pulse Detection Circuitry is independent of the DTL / TTL Switch Position.