LD-2

PENCILBOX™
LOGIC DESIGNER

INSTRUCTION MANUAL

80-01-0387
5/87

E&L Instruments
An Interplex Electronics Company
70 Fulton Terrace, P.O. Box 1942
New Haven, Connecticut 06512

WARNING

FEDERAL REGULATION (PART 15 OF FCC RULES) PROHIBITS THE USE OF COMPUTING EQUIPMENT WHICH CREATES RADIO OR TV INTERFERENCE

Interplex Electronics specifically warns the user of this instrument that it is intended for use in a classroom or laboratory environment for the purpose of learning and experimentation. When building experimental circuits, it may emit interference that will effect radio and television reception and the user may be required to stop operation until the interference problem is corrected. Home use of this equipment is discouraged since the likelihood of interference is increased by the close proximity of neighbors.

CORRECTIVE MEASURES:

Interference can be reduced by the following practices.

1) Install a commercially built RFI power filter in the power line at the point where the cord enters the unit.

2) Avoid long wires. They act as antennas.

3) If long wires must be used, use shielded cables or twisted pairs which are properly grounded and terminated.

By

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SPECIFICATIONS

POWER SUPPLIES:

+12 Volts ± 5% 200mA max.
-12 Volts ± 5% 200mA max.
+5 Volts ± 5% 250mA max.

TTL/CMOS OPERATION

Selectable output voltage of Clock, Pulsers, Logic Switches. Input voltage thresholds of Seven Segment Displays, Logic Indicators and Vcc tie point between 5 volts, TTL, and 12 volts, CMOS.

CLOCK:

1Hz ± 20%
1kHz ± 20%
100kHz ± 20%

Also user variable with external capacitor.

LOGIC "1" OUTPUT CURRENT:

2mA @ 4.0V min. (5V/TTL)
4mA @ 11.0V min. (12V/CMOS)

LOGIC "0" OUTPUT CURRENT:

2mA @ 0.1V max (5V/TTL)
5mA @ 0.1V max (12V/CMOS)

PULSERS:

Two fully debounced pushbuttons with logic true and complementary outputs.

LOGIC "1" OUTPUT CURRENT:

2mA @ 2.5V min. (5V/TTL)
2mA @ 11.0V min. (12V/CMOS)

LOGIC "0" OUTPUT CURRENT:

2mA @ 0.4V max. (5V/TTL)
5mA @ 0.4V max. (12V/CMOS)

LOGIC SWITCHES:

Eight SPDT switches select output of Vcc or ground (0 volts). Output current, all cases: 200mA max.

LOGIC INDICATORS:

Eight LEDs buffered by two 4-bit latches with separate enables. Input Impedance, all inputs: 100k ohms.

SEVEN SEGMENT DISPLAYS:

Two BCD-input seven segment displays with separate Display Enable (DE), Latch Enable (LE), and Lamp Test ($\overline{LT}$) inputs. Input Impedance, all inputs: 100k ohms.

CONNECTORS:

All functions are permanently tied to three solderless tie point connectors. Each tie point has two solderless connection points. Gnd (ground), +5 volts, Vcc, and Clock Out have four connection points each. All tie point functions are marked on the front panel.

BNCs:

Two BNC connectors with the shells tied to ground and the pins connected to adjacent single tie points.

BREADBOARDING:

One E & L Instruments SK-10 Solderless Breadboarding Socket is permanently attached to the unit. The SK-10 can accommodate up to eight 14-pin DIP ICs with 4 tie points per pin plus 8 power rails with 25 tie points each.

PHYSICAL:

Length	10 in.	25.4 cm.
Width	7.5 in.	19.05 cm.
Height	2.6 in.	6.6 cm.

WEIGHT:

LD-2 only	1 lb. 6 oz.	624 grms.
LD-2 with charger	2 lb. 13 oz.	1.28 kg.

INTRODUCTION/DESCRIPTION

The LD-2 Pencil Box is an instrument capable of satisfying the many requirements arising in the design and study of analog and digital circuitry. The instrument contains three integral power supplies and input/output devices that simplify the construction of a wide range of circuits. Typical circuits that can be built on the LD-2 include, operational amplifiers, comparators, A to D converters, gates and counters. The LD-2 can even interface directly to a microprocessor.

The LD-2 contains eight LED logic indicators, eight logic switches and two BCD - input seven-segment displays. It also contains a clock with three switch-selectable output frequencies, and three power supplies. The power supplies are +12 volts, +5 volts and -12 volts.

The logic indicators on the LD-2 can serve two functions. They may be used either as eight "real time" logic probes or as two latchable four-bit logic indicators.

All of the LD-2 functions mentioned above are internally connected to three solderless interconnect sockets with two tie points for each signal. In addition, an SK-10 Solderless Bread-boarding Socket is permanently attached to the unit. It provides a convenient work area for the circuitry being designed or studied. All sockets allow insertion of components or wires up to 22 gauge. For components with larger diameter leads use E & L's BP-24 Adapter Pins, which can accept wire leads up to 16 gauge.

A wall adapter type power supply is used to generate the regulated voltages used on the LD-2. Power supply connections to the instrument are made via the five (5) pin DIN connector.

The LD-2 is housed in a durable and attractive case with a hinged protective cover. This makes the unit portable and stackable for storage purposes.

LOCATION AND DESCRIPTION OF OPERATING CONTROLS AND MAJOR COMPONENTS

In order to properly use the full capabilities of the LD-2, it is highly recommended that the user become familiar with the controls associated with this instrument (See Figure 1).

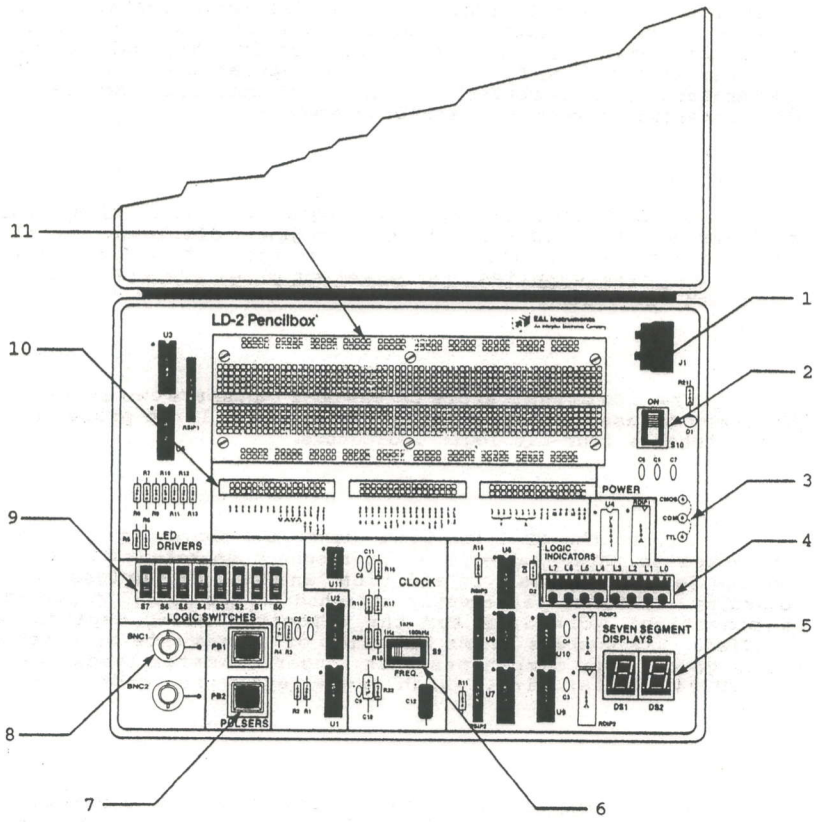


FIGURE 1. Location and description of operating controls.

POWER RECEPTACLE (1)

Five (5) pin DIN type receptacle power supply connection.

Power Switch (2)

Push Power Switch S10 up to apply power to the LD-2, move switch back to turn power off. LED D1 lights to show power ON condition.

CMOS/TTL Switch (3)

Selector S8, is made up of three individual breadboarding tie points, and determines the operating voltage of the LD-2 circuitry. For 12 volt operation, install a jumper wire from the center tie point to the upper tie point labeled CMOS. In this condition, the output amplitude of the Logic Switches, Pulsers, Clock, and Vcc tie point is 12 volts, and the input thresholds to the Seven-Segment displays and Logic Indicators are set to 12 volts CMOS levels.

For 5 volt operation, install the jumper wire from the center tie point to the lower tie point labeled TTL. This will cause the output amplitude of the Logic Switches, Pulsers, Clock, and Vcc tie point to be 5 volts, and the input thresholds to the Seven Segment Displays and Logic Indicators to be set to levels usable for TTL, or CMOS operating at 5 volts.

CAUTION

A jumper must be installed selecting either the CMOS or TTL position before power is applied, and power must be removed when it is desired to change the selection.

Logic Indicators (4)

The eight LEDS L0-L7, are used for indicating logic states of circuit points. A logic 1 on a logic indicator input will light its corresponding LED. In addition, the logic indications can be latched to freeze the states shown; a high-to-low transition on Clock $\overline{X}$ will latch LEDs L0 through L3, and a high-to-low transition on Clock $\overline{Y}$ will latch LEDs L4 through L7. While Clock $\overline{X}$ or Clock $\overline{Y}$ remain low, the logic indications will remain latched; bringing these points high will restore the indicators to a real-time display.

Seven-Segment Displays (5)

DS1 and DS2 are two independent seven-segment numeric displays. These are enabled, or turned on, by applying a logic 1 to the Display Enable tie-points DS1DE for DS1, DS2DE for DS2. When enabled, the displays will show a zero if no other inputs are present. Numbers are displayed by applying a logic 1 to the D, C, B and A tie-points in BCD, from 0000 to 1001. Input of 1010 or greater will cause the display to blank. The number displayed can be latched by a low-to-high transition on the LE (Latch Enable) input. This latched condition will exist as long as a logic 1 is maintained; when LE is returned to a logic 0, or low, the displays will be restored to their real time status. At any time the displays are enabled,a Lamp Test can be performed by applying a logic 0 to the $\overline{LT}$ tie point associated with the display. This will confirm the proper functioning of each display by lighting all LED segments.

Frequency Switch (6)

The three position frequency switch, S9, is used to select the output frequency of the clock. This output is available as either 1Hz, 1kHz, or 100kHz. The Clock Out amplitude is dependent upon the jumper installed in the CMOS/TTL selector S8, being 12 volts in the CMOS position and 5 volts in the TTL position. Frequency can also be changed by inserting a capacitor in the EXT CAP tie points. Some representative capacitors and their effect on a frequency are shown in Table 1.

	External Capacitor				
Freq. Switch Setting	0.001 μF	0.01 μF	0.1 μF	1.0 μF	10 μF
1Hz	1Hz	1Hz	0.91Hz	0.5Hz	0.091Hz
1kHz	500Hz	90.9Hz	9.9Hz	1Hz	0.1Hz
100kHz	50 kHz	9.09kHz	990Hz	100Hz	10Hz

Resulting Output Frequency

TABLE 1. Output frequency vs external capacitor value

Pulsers (7)

Pulsers PB1 and PB2 are two fully debounced pushbuttons with true and complementary outputs. These outputs are made available on the tie-point connector as PB1 ⎍, PB1 ⎍, PB2 ⎍, and PB2 ⎍. The PB1 output will be at a logic 1 while PB1 is not pressed, will go to a logic 0 when the switch is pressed,

and return to a logic 1 when the switch is released. The PB1 provides the complement of the above, that is,the point will be at a logic 0 while the switch is not pressed, will go to a logic 1 while the switch is pressed, and return to a logic 0 when the switch is released. The operation of PB2 is identical. In all cases, the logic 1 value is dependent upon the jumper installed in the CMOS/TTL selector, being 12 volts in the CMOS position and 5 volts in the TTL position.

BNCS (8)

Two additional connectors, BNC 1 and BNC 2, are provided to simplify input and output interfacing to the LD-2. The shells of both BNCs are connected to ground, while the pins of each individual BNC are connected to adjacent single tie points which can be wired to the solderless breadboard using jumper wires.

Logic Switches (9)

Eight SPDT logic switches S0 to S7 are provided with outputs at the connector tie points. These switches set a logic 1 to corresponding tie points when pushed up, and a logic 0 when pulled back. The logic 1 output voltage is dependent upon the jumper installed in the CMOS/TTL selector, being 12 volts in the CMOS position and 5 volts in the TTL position.

Connectors (10)

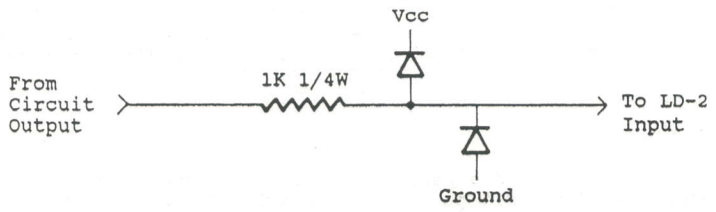
All functions are permanently tied to these three tie point connectors. Each tie point has two solderless connection points.

Solderless Breadboard (11)

The Solderless Breadboard, SK-10 accommodates up to eight 14-pin DIP ICs with 4 tie points per pin plus 8 power rails with 25 tie points each.

OPERATING PRECAUTIONS

The Logic Indicators and Seven-Segment Displays are intended for use only with digital signal inputs having voltage levels of Vcc or ground. It is, therefore, recommended that all interfacing be done with digital circuitry operating from the Vcc tie points. Exceeding Vcc, (12 volts with the CMOS/TTL selector jumpered to the CMOS position, 5 volts with the jumper in the TTL position) at any input will cause circuit damage to the LD-2, as will input voltages below ground. If necessary, input protection can be constructed on the SK10 Solderless Breadboarding Socket. An example of protection circuitry is shown in Figure 2. This circuit will protect any input over the voltage range of -15 volts to +20 volts without affecting input thresholds.



Diodes - any silicon diode 15mA or greater. Repeat this circuit for each input.

FIGURE 2. LD-2 input protection.

CHECKING OUT THE LD-2

To check out the LD-2 the following equipment is required.

1. A dual-trace oscilloscope, 10MHz bandwidth minimum.
2. DVM, 3 1/2 digit.

> **CAUTION**
>
> A jumper must be installed in selector S8 from center tie point to either the TTL or CMOS position before turning on power. Power must also be removed each time the position of this jumper is changed.

Procedure

Plug 5-pin DIN connector from wall adapter into J1 on the LD-2. Plug wall-mount adapter into outlet. Turn LD-2 Power switch to ON: LED D1 will light.

Step A.

Using an oscilloscope or a DVM, measure the power supply voltages present on the tie point connector:

1. +12 should read between +11.4 volts and +12.6 volts.
2. +5 should read between +4.75 volts and +5.25 volts.
3. -12 should read between -11.4 volts and -12.6 volts.
4. Vcc should read between:

   a. +11.4 volts and +12.6 volts with the CMOS/TTL switch in the CMOS position.
   b. +4.75 volts and +5.25 volts with the CMOS/TTL switch in the TTL position.

Step B.

Using an oscilloscope, measure the output frequency and amplitude of the clock out signal.

1. Set Freq switch to 1Hz.

   a. Frequency should be between 0.8Hz and 1.2Hz.
   b. Amplitude should be the same as Vcc levels, that is, +12volts with the CMOS/TTL selector jumpered to the CMOS position, and +5 volts with the CMOS/TTL selector jumpered to the TTL position.

2. Set Freq switch to 1kHz.

   a. Frequency should be between 800Hz and 1.2kHz.
   b. Amplitude should be +12 volts in CMOS, +5 volts in TTL.

3. Set Freq switch to 100kHz

   a. Frequency should be between 80kHz and 120kHz.
   b. Amplitude should be +12 volts in CMOS, +5 volts in TTL.

4. In all cases, duty cycle should be between 40% and 60%

Step C.

Use a jumper wire to test the Logic Indicators as follows:

1. Jumper CMOS/TTL selector to CMOS.
2. Observe that all 8 LEDS are off.
3. Connect a jumper wire between the Vcc tie point and the L0 tie point. L0 should light, all other LEDs should remain off.
4. Move the jumper wire from L0 to L1.
   L1 should light, all other LEDs should remain off.
5. Repeat these steps for L2 through L7.

Step D.

Use jumper wires to test the Seven-Segment Displays as follows:

1. Connect a jumper between DS1DE and +12 V.
   DS1 should light, showing a 0.
2. Connect a jumper between DS1$\overline{LT}$ and GND.
   All segments of DS1 should light.
3. Disconnect the jumper between DS1$\overline{LT}$ and GND.
   DS1 should again display a 0.
4. Jumper between DS1A and Vcc.
   A numeral 1 should be displayed on DS1.
5. Move the jumper from DS1A to DS1B.
   A 2 should be displayed.
6. Move the jumper from DS1B to DS1C.
   A 4 should be displayed.
7. Move the jumper from DS1C to DS1D.
   An 8 should be displayed.
8. Leaving the jumper in DS1D, connect another jumper from DS1LE to Vcc.
   The 8 should remain on.
9. Remove the jumper from DS1D.
   The 8 should remain on.
10. Remove the jumper from DS1LE.
    The display should return to 0.
11. Repeat steps 1-10 for DS2.

Step E.

Test the Pulsers by jumpering to L7 as follows:

1. Connect a jumper wire from PB1 ⊓⊔⊓ to L7
   a. Logic Indicator L7 will be lit while Pulser PB1 is not pressed.
   b. Pressing PB1 causes L7 to extinguish.
   c. Releasing PB1 causes L7 to relight.
2. Move the jumper wire from PB1 ⊓⊔⊓ to PB1 ⊔⊓⊔
   a. Logic Indicator L7 will not be lit while PB1 is not pressed.
   b. Pressing PB1 causes L7 to light
   c. Releasing PB1 causes L7 to extinguish
3. Repeat the above steps for PB2

Step F.

Test the Logic Switches by jumpering them to the Logic Indicators as follows:

1. Jumper S0 to L0, S1 to L1, and so on, through S7 to L7
2. Alternately move switches S0 through S7 up and back. The LED corresponding to each switch will light when the switch is up, and extinguish when the switch is down.
3. Leave all jumpers connected for the Latch test which follows.

Step G.

Test the Logic Indicator Latches as follows:

1. If not already accomplished, jumper the Logic Switches to the Logic Indicators as described in Step F (1).
2. Move all switches to the up position.
   All LEDS should light.
3. Connect jumpers from Clock $\overline{X}$ to GND and Clock $\overline{Y}$ to GND.
   All LEDs should remain lit.
4. Move all switches from the up to the down position.
   All LEDs should remain lit.
5. Remove the jumper from Clock $\overline{X}$.
   LEDs L0 through L3 should extinguish.
   LEDs L4 through L7 should remain lit.
6. Remove the jumper from Clock $\overline{Y}$.
   LEDs L0 through L3 should remain out.
   LEDs L4 through L7 should extinguish.

Step H.

Remove all remaining wires, except CMOS/TTL selector jumper.

All displays should be extinguished.

Step I.

Turn the Power Switch OFF.

This completes the checkout procedure.

08/18/86

INTERPLEX ELECTRONICS, INC.

BILL OF MATERIAL LISTING

BOM # 325-1802 LD-2 PENCILBOX 115V

COMPONENT	DESCRIPTION	QTY	REFERENCE DESIGNATORS
17-01-0002	BOM REV C	1	
02-05-0447	LD-2 PCB ASSEMBLY		
95-01-0246	LD-2 PCB	1	
37-01-1045	CCRES 1/4W 100K OHM 5%	14	R1-3, 5-15
37-01-1055	CCRES 1/4W 1MEG OHM 5%	1	R4
37-01-4715	CCRES 1/4W 470 OHM 5%	4	R16, 19, 21, 22
37-01-3335	CCRES 1/4W 33K OHM 5%	1	R17
37-01-6845	CCRES 1/4W 680K OHM 5%	1	R18
37-01-6225	CCRES 1/4W 6.2K OHM 5%	1	R20
37-08-0003	100K COM SIP 9 RES	3	RSIP 1-3
37-08-0006	33J OHM 8 RES DIP	3	RDIP 1-3
08-04-0104	CER CAP .1MFD 50V	9	C1-8, 11
08-02-0009	TANTCAP-1UF 10% 35V	1	C9
08-06-0011	MYLCAP.001MFD 100V 10%	1	C10
08-03-0226	ECAP 22UF 16V AX LD	1	C12
44-01-0112	4013 DUAL D FLI	1	V1
44-01-0063	4049AE HEX BUFF	1	U2
44-01-0059	RCA CD4042AE	2	U3,5
44-01-0302	ULN2031A DARTON ARRAY	1	U4
44-01-0041	IC CD-4010	3	U6-8
44-01-0008	IC CD 4511	2	U9, 10
44-01-0148	ICM7555IPA	1	U11
10-02-0007	LED GI #MV5075C	1	D1
10-01-0995	IN995 DIODE	1	D2
10-03-0005	DIOD HP5082-7760 736	2	DS1, 2
40-03-0029	SPST SLIDE ESCORT	8	SD-8
94-05-0023	LENS LD-2	1	
40-03-0028	3PDT ALCO(SLS-230 PC)	1	S9
20-02-0007	8PIN DIP SKT COM STD	1	
40-03-0027	4PDT SLDE ALCO MSS4200	1	S10
20-02-0004	16 PIN DIP SKT STD	9	
20-02-0014	14 PIN DIP SKT STD.	1	
40-04-0025	SPST PC MNT MOM PB MDP	2	PB1,2
20-03-0010	BNC W/NUT/INT TOTH WSR	2	
20-03-0192	5PN DIN PC MT,RGHT AGL	1	J1
20-03-0140	DP-25 SRDBDNG PIN R/D	5	
10-02-0019	LED ARRAY-4 PER BAR	2	LD-7
02-02-0016	IF-2X-16 PROTO-STRIP	3	
02-03-0023	UBS-10J SOCKET SA	1	
34-92-2210	BROWN 1.0" WIRE	15	
02-05-0448	LD-2 CASE ASSEMBLY		
94-03-0088	HSNG AIRMLD RH 2 3/8	1	
92-01-0006	RUBBER FOOT CTB	4	
86-10-0031	SPACER 5-32X1 118	4	