THE LOGICAL SERIES
MODULE TWO

DIGITAL ELECTRONICS

INSTRUCTOR'S GUIDE

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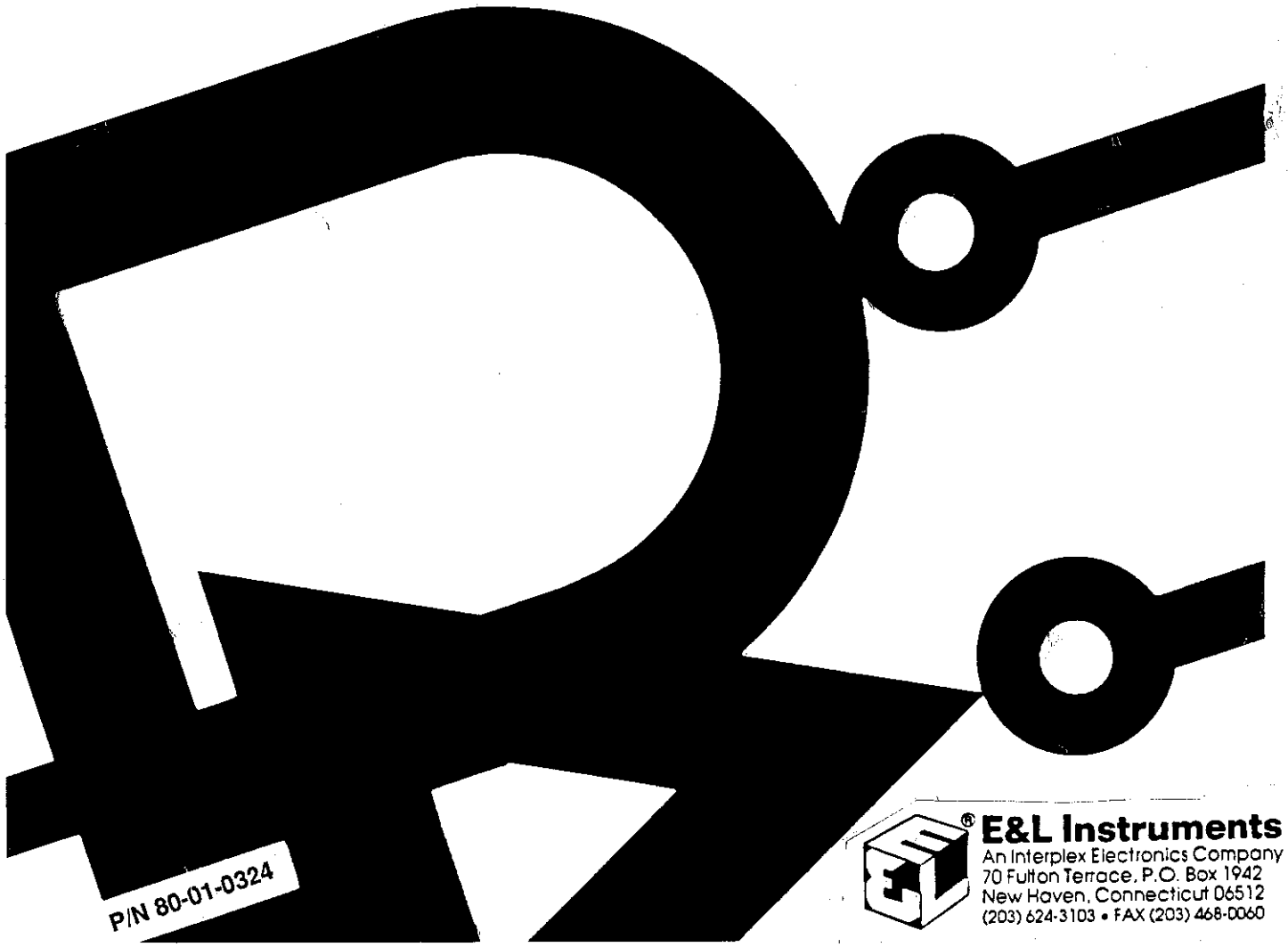
PRESTON BARBER



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INTRODUCTION

Thank you for purchasing and using this Digital Electronics program. The materials in this course were carefully chosen and organized with the intent of teaching a modern course in digital techniques. Both the authors and Interplex Electronics feel the method of course instruction emphasizes both hands-on experience and detailed theory for an effective presentation of material. We are certain you will find this course effective, timely and thorough.

Instructor's Guide for Digital Electronics

CHAPTER 1
INTRODUCTORY CONCEPTS

1.1 Objectives

After completing this chapter the student should be able to:

- Distinguish between digital and analog signals
- Discuss the use of 1s and 0s to represent quantity or condition
- Represent binary quantities
- Explain operation of a simple digital circuit

1.2 Questions and Answers

1. Explain the difference between digital and analog signals.
   Answer: Analog signals are continuous. Digital signals have discrete logic levels or states.

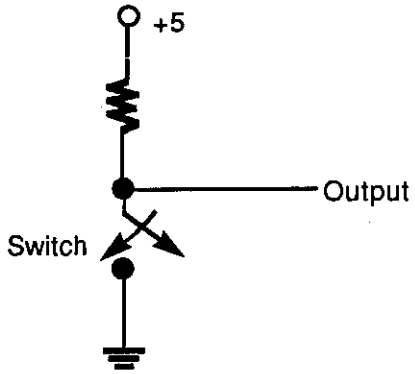
2. What states can a bit be in ?
   Answer: A binary digit can be in the logic 0 or logic 1 (TRUE or FALSE, ON or OFF, and LO or HI are acceptable answers) state.

3. What numbers can a bit represent ?
   Answer: A bit can represent the numbers 1 and 0.

4. Draw the schematic of a simple digital switch. Why do these switches seldom appear as shown ?(See Figure 1-1, page 2).

FIGURE 1-1. Simple Digital Switch

Answer:



The contacts of the mechanical switch will bounce between states when the switch is activated. This can cause false triggering in logic circuits connected to the switch.

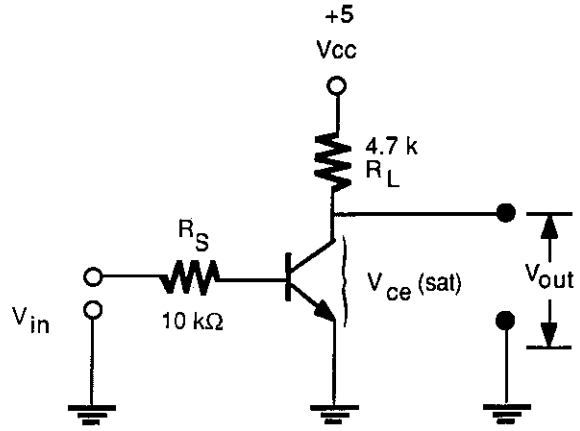
5. Who constructed the first integrated circuit ?
Answer: Texas Instruments constructed the first integrated circuit.

6. Name some qualities of an analog circuit.
Answer: Analog circuits feature active devices such as a transistor operated in the linear region. The circuits are designed to amplify a signal with minimal distortion. The output range is limited so that the transistor is not driven into saturation.

7. Name some qualities of a digital circuit.
Answer: A digital circuit is designed to switch quickly between the allowed digital states. A transistor operated in the saturated region forms a basic digital circuit. The output is at Vcc or "ground" except for brief switching times.

8. Draw the schematic for a simple BJT digital inverter. Explain it's operation.
Answer:

FIGURE 1-2. BJT Inverter



The circuit is operated in the saturated region.When the input is Vcc, the circuit is saturated if Ic >> (beta) X Ib. The output is a low voltage (0.2-0.6 V for a silicon BJT). When the input is near ground, the transistor is cut off and the output is Vcc.

9. Explain what an integrated circuit is.
   Answer: An integrated circuit features multiple transistors on a single piece of silicon.

1.3 Labs

This chapter has no laboratory.

CHAPTER 2
NUMBER SYSTEMS AND CODES

2.1 Objectives

Upon completion of this chapter the student should be able to:

- Use and explain the binary number system.
- Convert from binary numbers to decimal numbers.
- Convert from decimal numbers to binary numbers.
- Use and explain the hexadecimal number system.
- Use and explain the octal number system.
- Use and explain the BCD code.
- Use and explain the ASCII code.

2.2 Questions and Answers

1. What is the radix of the binary number system?
   Answer: The binary radix is two.

2. What is the common name for the radix ten number system?
   Answer: The common name is decimal.

3. Which number system can have a weight of B ?
   Answer: The hexadecimal number system can have a weight of B.

4. How many bits are required to represent an Octal digit?
Answer: Three bits are required to represent an octal digit.

5. What is the common name for the radix 16 number system.
Answer: The common name is hexadecimal or hex.

6. Convert decimal 122 to binary.
Answer:

Process	Remainder
122/2 = 61	0
61/2 = 30	1
30/2 = 15	0
15/2 = 7	1
7/2 = 3	1
3/2 = 1	1
1/2 = 0	1

122 decimal = 1111010 binary

7. Convert hexadecimal EF to binary.
Answer: EF hex = 1110 1111 binary

8. Convert hexadecimal EF to decimal.
Answer: From 7, EF = 1110 1111
1110 1111 = 128 + 64 + 32 + 8 + 4 + 2 + 1 = 239 decimal

9. Air Force Work unit codes are a radix 34 system. How many parts can be in a system which has a three digit work unit code?
Answer: The number of parts is 39304 which is 34 cubed.

10. Convert decimal 125 to octal.
Answer: First convert to binary.

Process	Remainder
125/2 = 62	1
62/2 = 31	0
31/2 = 15	1
15/2 = 7	1
7/2 = 3	1
3/2 = 1	1
1/2 = 0	1

125 decimal = 1111101 binary
1 111 101 binary = 175 octal

11. Convert octal 33 to hexadecimal.
    Answer: 33 octal = 011 011 binary = 01 1011 binary = 1B

12. Convert A0 hexadecimal to decimal.
    Answer: A0 hex = (A x 16) + (0) = 160 decimal

13. What binary code will be required to force an ASCII device to ring the bell?
    Answer: The ASCII code for the bell is 0000111 binary

14. What is the hexadecimal value of ASCII A?
    Answer: ASCII A = 41 hex

15. Convert 9 decimal to ASCII.
    Answer: 9 decimal = 39 hex = ASCII 11 1001

2.3 Labs

There are no labs for chapter two.

CHAPTER 3
LOGIC GATES AND BOOLEAN ALGEBRA

3.1 Objectives

Upon completion of this chapter the student should be able to:

- Identify Boolean variables
- Explain the basic operations of Boolean Algebra
- Identify and write Boolean equations
- Use logic circuits to implement Boolean equations

3.2 Questions and Answers

1. Who first formulated Boolean algebra ?
   Answer: George Boole.

2. What is the practical use of Boolean algebra ?
   Answer: Boolean algebra allows us to resolve logical propositions by correctly answering a number of true/false questions. It also allows us to express logical propositions as mathematics equations.

3. What are the three basic operations allowed in Boolean algebra ?
   Answer: The three basic boolean operations are: NOT (or complement), AND (or multiplication), OR (or addition).

4. How many variables does the AND function operate on ?
Answer: The AND function operates on 2 or more variables.

5. How many variables does the NOT function operate on ?
Answer: The NOT function operates on one variable.

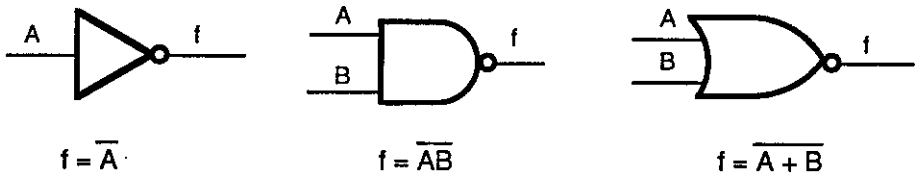
6. What is a truth table ?
Answer: A truth table lists all possible combinations of states of independent variables and the corresponding state of the dependent variable.

7. Show the truth table for the NAND function.
Answer:

A	B	Y
0	0	1
1	0	1
0	1	1
1	1	0

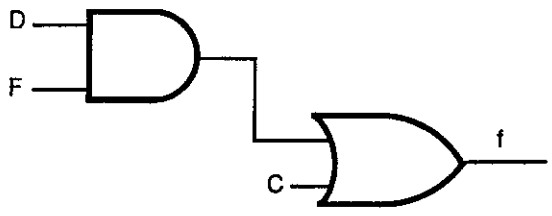
8. Write the schematic symbols for the three basic logic operations.
Answer:

FIGURE 3-1. Basic Logic Symbols



9. Show the schematic of a circuit that will perform the operations in the following logical equation: f = C+DF.
Answer:

FIGURE 3-2. Schematic f = C+DF



10. Show a truth table for the equation from question nine.
Answer:

C	D	F	f
0	0	0	0
0	0	1	0
0	1	0	0
1	0	0	1

C	D	F	f
0	1	1	1
1	0	1	1
1	1	0	1
1	1	1	1

11. Name the combinational logic circuits ?
Answer: The combinational logic circuits are the AND, OR, and NOT gates.

12. What are combinational logic circuits used for ?
Answer: Combinational logic circuits are used to implement and solve boolean equations. Combinational logic circuits are used in decision making.

13. Why have digital integrated circuits become so popular ?
Answer: Digital integrated circuits provide an economical, compact, rugged and reliable method of implementing boolean equations.

3.3 Labs

3.3.1 Laboratory 3.1 THE NOT GATE

3.3.1.1 Results

Step 8:

L1	L2
ON	OFF
OFF	ON

3.3.1.2 Questions and Answers Lab 3.1

1) Construct a truth table for the 74LS04 hex inverter.

Answer:

A	Y
1	0
0	1

Note: A = S1 = L1 and Y = L2

2) Why is the 7404 called a hex inverter ? (hint: look at the basing diagram)
Answer: The device is named for the six logic inverters or NOT gates which it contains.

3) Are the lights L1 and L2 ever on simultaneously ?
Answer: Strictly speaking, both lights are on when the input undergoes a LO to HI transition for an amount of time equal to the device gate delay. The students have yet to learn about gate delay. To the naked eye, both LEDs are never on at once, hence the correct answer is NO.

3.3.2 Laboratory 3.2 THE AND GATE

3.3.2.1 Results

Step 10:

S1	S2	L3
0	0	0
1	0	0
0	1	0
1	1	1

3.3.3 Laboratory 3.3 THE OR GATE

3.3.3.1 Results

Step 10:

S1	S2	L3
0	0	0
1	0	1
0	1	1
1	1	1

3.3.4 Laboratory 3.4 THE NAND GATE

3.3.4.1 Results

Step 10:

S1	S2	L3
0	0	1
1	0	1
0	1	1
1	1	0

3.3.5 Laboratory 3.5 THE NOR GATE

3.3.5.1 Results

S2	S3	L1
0	0	1
1	0	0
0	1	0
1	1	0

3.3.6 Laboratory 3.6 USE OF NAND AND NOR GATES

3.3.6.1 Results

Step 11:

S2	S3	L4
0	0	0
1	0	1
0	1	1
1	1	1

This is the logical OR function.

Step 17:

S2	S3	L4
0	0	1
1	0	1
0	1	1
1	1	0

This is the logical NAND function.

Step 18:

S2	S3	L6
0	0	0
1	0	0
0	1	0
1	1	1

This is the logical AND function.

Step 19:

L4	L6
1	0
0	1

3.3.6.2 Questions and Answers

1) Which logic function is performed by the circuit observed in step 19 ?
Answer: The circuit is an inverter.

2) All of the basic Boolean functions have been demonstrated using the 74LS02 quad two-input NOR gate. Design a circuit to implement the basic Boolean functions. Use the 74LS00 quad two-input NAND as your IC. Describe which gate combinations perform which Boolean functions. Breadboard your circuit and check it's operation.
Answer:

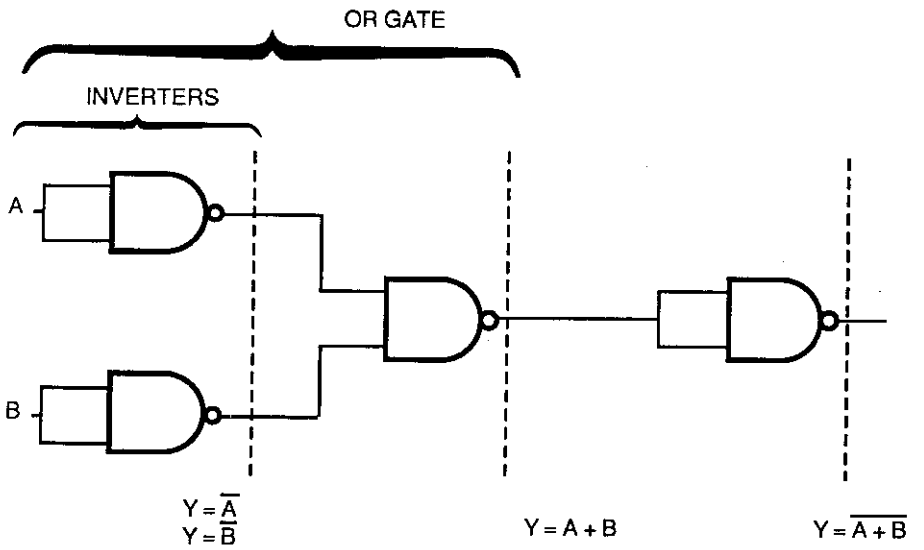


FIGURE 3-3. Schematic for Question 2

- gate 4 is an inverter
- gates 3 and 4 form an AND gate
- gate 3 is a NAND gate
- gates 1, 2 and 3 form an OR gate.
- All four gates function as a NOR gate.

CHAPTER 4
COMBINATIONAL LOGIC CIRCUITS

4.1 Objectives

Upon completion of this chapter the student should be able to:

- Simplify logic expressions.
- Simplify logic circuits.
- Use the Karnaugh map to simplify logic circuits and expressions.

4.2 Questions and Answers

1. Determine the simplified logic equation for each of the K-maps in Figure 4-14.
   Answer:
   a. $\overline{A}\overline{B} + A\overline{B}\overline{D}$
   b. $B\overline{C} + B\overline{D}$
   c. A

2. Write the original equations used to form the K-maps of Figure 4-14.
   Answer:
   a. $\overline{A}B\overline{C}\overline{D} + \overline{A}BC\overline{D} + \overline{A}BCD + A\overline{B}\overline{C}\overline{D} + A\overline{B}C\overline{D} + AB\overline{C}\overline{D}$
   b. $\overline{A}B\overline{C}\overline{D} + \overline{A}BC\overline{D} + \overline{A}BCD + A\overline{B}\overline{C}\overline{D} + A\overline{B}CD + ABCD$
   c. $AB\overline{C} + ABC + A\overline{B}\overline{C} + A\overline{B}C$

3. Simplify the equations in question 2 using Boolean algebra-show all steps.

Answer:

a. $(\overline{A}\overline{B}\overline{C}(\overline{D}+D)) + (\overline{A}\overline{B}C(\overline{D}+D)) + (\overline{A}\overline{B}\overline{D}(\overline{C}+C))$

$\overline{A}\overline{B}\overline{C} + \overline{A}\overline{B}C + \overline{A}\overline{B}\overline{D}$

$(\overline{A}\overline{B}(\overline{C}+C)) + \overline{A}\overline{B}\overline{D}$

b. $(\overline{A}\overline{B}\overline{C}(\overline{D}+D)) + (A\overline{B}\overline{C}(\overline{D}+D)) + (B\overline{C}\overline{D}(\overline{A}+A))$

$(B\overline{C}(\overline{A}+A)) + B\overline{C}\overline{D}$

$B\overline{C} + BC\overline{D} = B(\overline{C}+C\overline{D}) = B(\overline{C}+\overline{D}) = B\overline{C} + B\overline{D}$

c. $AB\overline{C} + ABC + A\overline{B}\overline{C} + A\overline{B}C$

$(AB(\overline{C}+C)) + (A\overline{B}(\overline{C}+C))$

$AB + A\overline{B} = A(\overline{B}+B) = A$

4. Sketch the outputs for the inputs shown in Figure 4-15.

Answer:

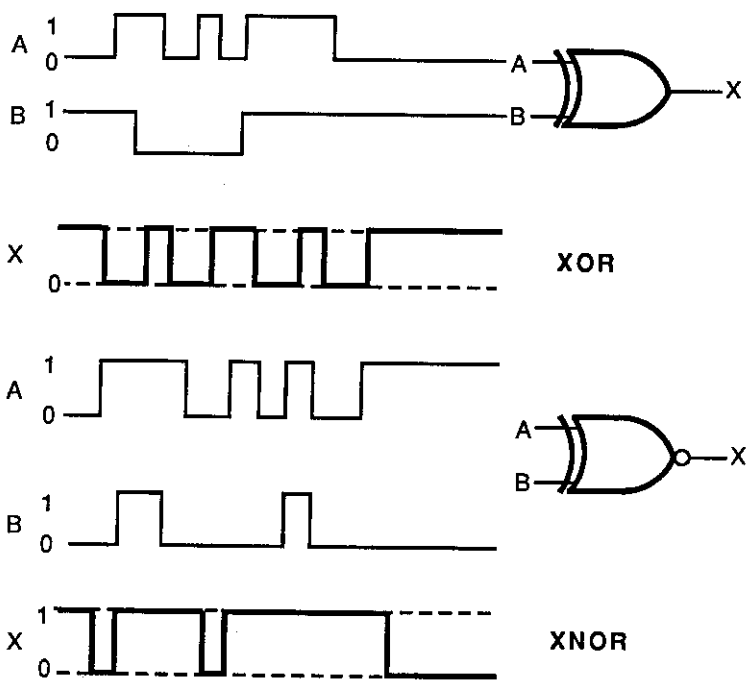


FIGURE 4-15. Outputs for XOR and XNOR Gates

5. In the space below, show how Exclusive OR and Exclusive NOR circuits are constructed from AND, OR and NOT gates.

Answer:

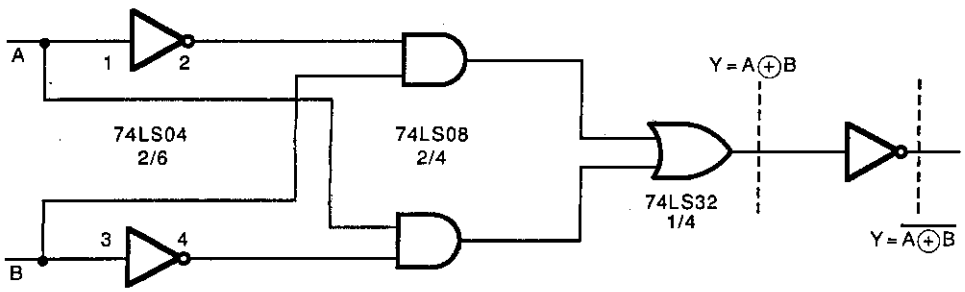


FIGURE 4-1. EXOR and EXNOR from Basic Gates

4.3 Labs

4.3.1 Lab 4.1 Minterm and Maxterm Truth Tables

4.3.1.1 Results

1. The logic equation for the minterm truth table is $Y = \overline{A}B$.

7. The truth table is:

S1	S2	L3
0	0	0
1	0	0
0	1	1
1	1	0

8. The maxterm truth table is:

A	B	Y
1	1	1
0	1	1
1	0	0
0	0	1

The product of sums form of the equation is:

$$Y = (\overline{A}+B)(\overline{A}+\overline{B})(A+B)$$

17. The truth table of this circuit is:

S1	S2	L3
0	0	0
1	0	0
0	1	1
1	1	0

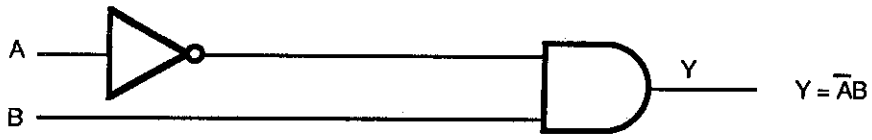
4.3.1.2 Questions and Answers

1. Compare the truth tables from steps 7 and 17. What do you notice about them ?
Answer: They are identical.

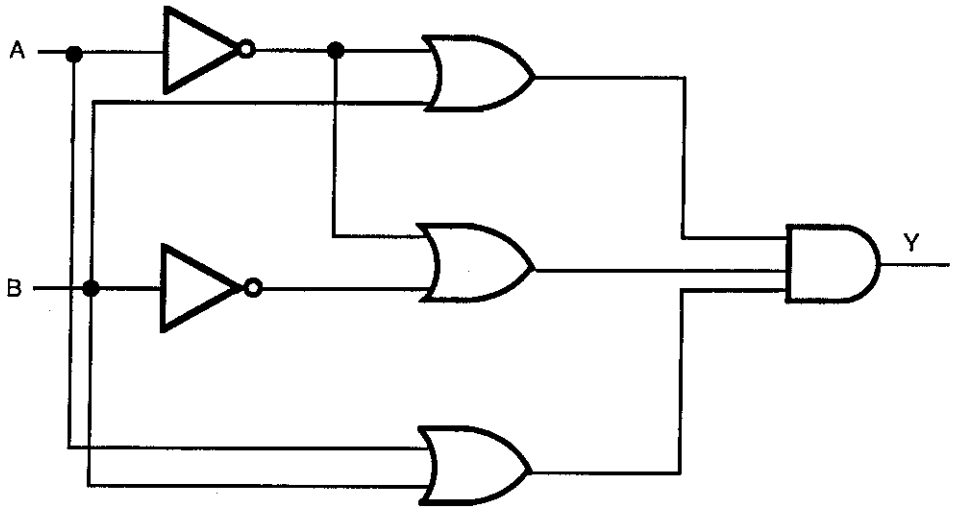
2. Draw schematic diagrams of the circuits that produced the truth tables in steps 7 and 17.
Answer:

FIGURE 4-2. Schematics Steps 7 and 17

Step 7



Step 17



3. Which circuit better performs this logic function ? (Step 7 or Step 17 ?) Why ?
Answer: The circuit from Step 7 uses fewer parts and interconnecting wires. It is the preferred circuit since it is less expensive and more reliable.

4.3.2 Lab 4.2 Simplifying Logic Circuits

4.3.2.1 Results

1. The sum of products form of the logic equation is:
$Y = \overline{A}\,\overline{B} + \overline{A}B + A\overline{B}$

10. The truth table is:
Answer:

S1	S2	L3
0	0	1
1	0	1
0	1	1
1	1	0

13. The K-map is:

	$\overline{A}$	A
$\overline{B}$	1	1
B	1	

FIGURE 4-3. K-Map for Step 13

14. The simplified logic equation for this map is: $Y = \overline{B} + \overline{A}$.

20. The truth table for this circuit is:

S1	S2	L3
0	0	1
1	0	1
0	1	1
1	1	0

4.3.2.2 Questions and Answers

1. What is the common name for the logic function displayed in the truth table in step 1?
   Answer: NAND

2. What do you notice about the truth tables resulting from steps 10 and 20 ?
   Answer: They are the same.

3. What do you call the simplified logic equation from the results of step 14 ?
   Answer: The maxterm form of the NAND.

4. Which of the circuits is better to use ? Why?
   Answer: The circuit of step 20 uses fewer components and has fewer interconnections. This circuit should be less expensive to construct and should operate more reliably. For these reasons the circuit of step 20 is preferred.

4.3.3 Lab 4.3 Decoders

4.3.3.1 Results

4. The truth table for this circuit is:

S1	S2	S3	L1
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

9. The table for this circuit is:

S2	S1	L0	L1	L2	L3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

4.3.3.2 Questions and Answers

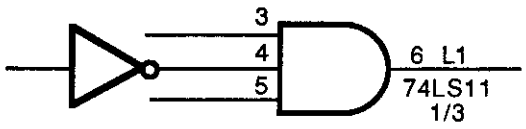
1. What binary number does the circuit from step 4 decode ?
   Answer: 111

2. Name one use of a circuit like the one in Figure 4-6.
   Answer: This circuit could be used as an address decoder for memory.

3. Explain the operation of the one of four decoder.
   Answer: Each AND gate decodes one of the possible four input numbers. The inputs are generated by the logic switches and inverters.

4. Design a circuit to decode 101 binary.
   Answer:

FIGURE 4-4. 101 Decoder



5. Circuits similar to the one of four decoder are used to convert from BCD to decimal. How many AND gates will be required to implement such a circuit ?
   Hint: Examine the schematic in Figure 4-7 (student text).
   Answer: 10 AND gates are required.

6. Why can't the logic equation from the truth table of step 9 be written as $y = \overline{A}\overline{B} + A\overline{B} + \overline{A}B + AB$?
Answer: The outputs are distinct, not common.

4.3.4 Lab

4.4 Encoders

4.3.4.1 Results

4. When PB1 is pressed L0 is turned ON.

5. When PB2 is pressed L1 is turned ON.

6. When S0 is OFF L0 and L1 are turned ON.

4.3.4.2 Questions and Answers

1. What does the circuit of step one do ?
Answer: This circuit encodes PB1, PB2, and S3 to a pair of bits.

4.3.5 Lab 4.5 EXOR Circuits

4.3.5.1 Results

5. The truth table for this circuit is:

S1	S2	L3
0	0	0
0	1	1
1	0	1
1	1	0

11. The truth table for this circuit is:

S1	S2	L3
0	0	0
1	0	1
0	1	1
1	1	0

4.3.5.2 Questions and Answers

1. Examine the truth tables from steps 1, 5, and 11. What do you notice about them ?
Answer: They are the same.

2. What math function does the EXOR gate perform ?
Answer: The EXOR gate is the simplest binary adder.

3. Which circuit is better to use, the one from step 3 or the one from step 9? Why?
Answer: The circuit of step 9 uses fewer parts and has fewer

interconnections. The circuit of step 9 is preferred since it is less expensive to build and more reliable.

4. Draw the Karnaugh map for the EXOR. Can this be reduced?
Answer:

FIGURE 4-5. EXOR K-Map

	$\overline{A}$	A
$\overline{B}$		1
B	1	

The circuit cannot be reduced further since all ones are on diagonals.

4.3.6 Lab 4.6 The EXNOR Circuit

4.3.6.1 Results

3. The truth table for this circuit is:
Answer:

S1	S2	L3
0	0	1
0	1	0
1	0	0
1	1	1

6. L3 is the complement of S1.

4.3.6.2 Questions and Answers

1. Write the EXNOR logic equation directly from the truth table.
Answer: $\overline{A}\overline{B} + AB = Y$

2. What function does the circuit of step five perform ?
Answer: The circuit is an inverter.

3. Make a Karnaugh map for the EXNOR function. Can this function be reduced ?

FIGURE 4-6. EXNOR K-Map

	$\overline{A}$	A
$\overline{B}$	1	
B		1

The circuit cannot be reduced since all ones are diagonal.

CHAPTER 5
FLIP-FLOPS

5.1 Objectives

Upon completion of this chapter the student should be able to:

- Define and describe the action of a flip-flop.
- Describe and implement a S-C (set-clear) flip-flop.
- Describe and implement a J-K flip-flop.
- Describe and implement a D flip-flop.
- Explain and use a T flip-flop
- Explain the difference between synchronous and asynchronous circuits.
- Describe some common applications of flip-flops.
- Explain what a one-shot is.

5.2 Questions and Answers

1. What is a flip-flop ?
   Answer: The flip-flop is a digital logic element used for storing binary data.

2. Draw the circuit diagram and schematic symbol for a S-C flip-flop. Explain the operation of this circuit.

Answer:

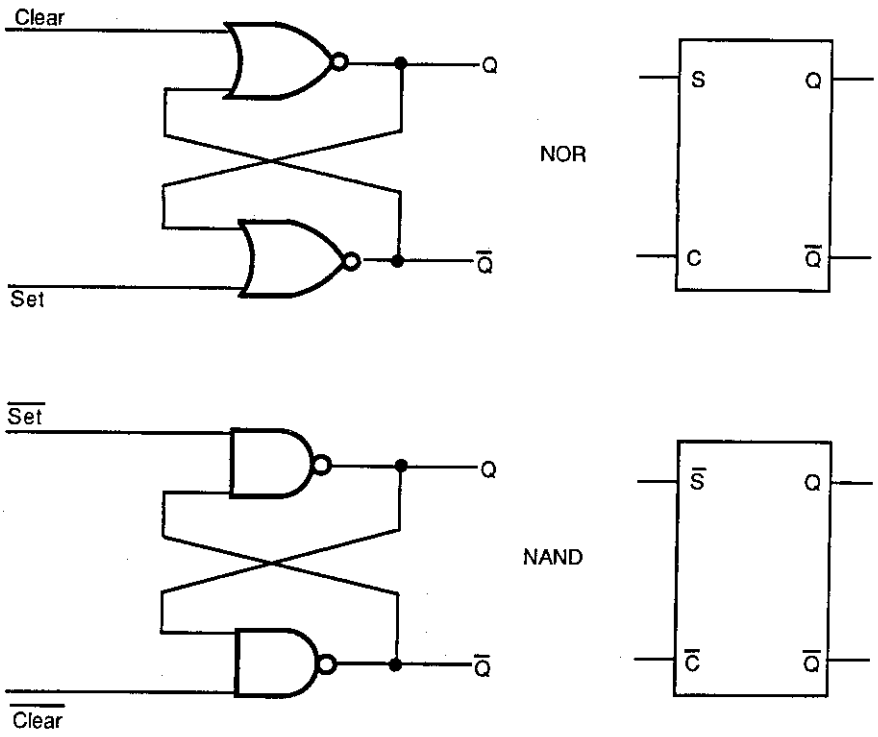


FIGURE 5-1. S-C Flip-Flop Circuit Diagram and Logic Symbol

The operation of the NOR S-C flip-flop is straightforward. Assume that initially the Set and Clear inputs and the Q output are all LO. If the Set input is forced HI while the Clear input is forced LO, the Q output will be forced to the HI state. The HI Q output causes the complement output to be LO. If the Set line now returns to LO, the Q output will remain HI as long as the Clear input is LO. The flip-flop can be cleared by bringing the Clear input HI while holding the Set input LO. This results in a LO on the Q output. The LO Q output results in a HI on the complement output. At this point the Clear input can return to the LO state and the flip-flop is cleared until the next Set command is received. The Clear and Set inputs should not be brought to the HI state at the same time. The operation of the NAND S-C flip-flop is similar except that a LO input is required to activate the inputs. The forbidden state of the NAND S-C flip-flop is both inputs LO.

3. Why are clock signals used in sequential logic circuits ?
Answer: Clock signals allow flip-flops to be chained together and still operate correctly even though the gates used to form the flip-flops have varying propagation delays and settling times.

4. What is the primary characteristic of sequential logic circuits?
Answer: The primary characteristic of sequential logic circuits is memory.

5. Name six types of flip-flops.
Answer: S-C, D, T, clocked S-C, clocked D, and J-K are six types of flip-flop.

6. What is a name for a flip-flop other than latch ?
Answer: Flip-flops are also known as bistable mulitvibrators.

7. What is a one-shot ?
Answer: A one-shot is a device with one stable output state. When a trigger pulse is received on the input a single pulse appears at the output.

8. Name an application of one-shots.
Answer: One shots are frequently used for contact debouncing.

9. Name two applications of J-K flip-flops.
Answer: J-K flip-flops are frequently used for counting and frequency division.

10. What is the maximum count that can be contained in a ripple counter made of three J-K flip-flops ?
Answer: Binary 111 is the maximum count for this type counter.

11. Would your answer to question 10 change for T flip-flops ? Why?
Answer: No the answer does not change. The counter is still a three bit counter and has a maximum count of binary 111.

5.3 Labs

5.3.1 Lab 5.1 Set-Clear Flip-flops

5.3.1.1 Results

3. The truth table for this circuit is:

S1	S2	L1	L2
1	1	0*	1*
0	1	1	0

S1	S2	L1	L2
1	0	0	1
1	1	x	x

* After initial power up. Other times the state is determined by which of S1 and S2 was last HI.
x Race condition. Both outputs appear LO.

7. The truth table for this circuit is:

S1	S2	L1	L2
1	1	0*	1*
0	1	1	0
1	0	0	1
0	0	x	x

* After initial power up. Other times the state is determined by which of S1 and S2 was last LO.
x Race condition. Both outputs appear HI.

5.3.1.2 Questions and Answers

1. Which states cause trouble for the NOR S-C FF ?
Answer: Both inputs HI causes a race condition in the NOR S-C flip-flop.

2. Which states cause trouble for the NAND S-C FF ?
Answer: Both inputs LO causes a race condition in the NAND S-C flip-flop.

3. What state should the inputs to a NOR S-C FF be in ?
Answer: Normally LO unless a change of state is desired.

4. What state should the inputs to a NAND S-C FF be in ?
Answer: Normally high unless a change of state is desired.

5.3.2 Lab 5.2 The D Latch

5.3.2.1 Results

3. The truth table for this circuit is:

S1	L1	L2
0	1	0
1	0	1

5. The truth table for this circuit is:

S1	L1	L2
0	0	1
1	1	0

5.3.2.2 Questions and Answers

1. What do you notice about the circuit of Figure 5-19 (student text) ? How could this circuit be simplified ?
   Answer: The Q output, L2, is always the same state as the input. The circuit could be replaced with a wire for the Q output and an inverter for the complement output.

2. How could the circuit of step 5 be constructed using only one IC ? Build a circuit to test your solution.
   Answer: The input is fed through an inverter to form the Q output. A direct wire from the input will form the complement output.

5.3.3 Lab 5.3 The Clocked Set-Clear Flip-flops

5.3.3.1 Results

3. L7 will flash on and off with a 50% duty cycle

5. The truth table for this circuit is :

PB2	S1	S2	L1	L2	
LHL	0	0	Q	$\overline{Q}$	no change from previous state
LHL	1	0	1	0	
LHL	0	1	0	1	
LHL	1	1	1	1	disallowed state

6. The inputs have no effect until the clock signal is pulsed.

5.3.3.2 Questions and Answers

1. Does adding the clock circuitry cure the inherent flaws of the S-C flip-flop circuit ? Explain.
   Answer: No the flip-flop still has a disallowed state.

2. When do the input signals have an effect on the output states?
   Answer: Inputs have no effect until the clock signal is pulsed.

5.3.4 Lab 5.4 The T Flip-flops

5.3.4.1 Results

3. The initial state of the latch is RESET.

4. The Q output will go through a complete cycle (LO to HI then back to LO) after 2 clock pulses.

6. The output frequency is one-half the clock frequency.

5.3.4.2 Questions and Answers

5.9.4 Questions

1. What effect does the T FF have on binary pulse trains ?
   Answer: The T FF divides the input clock frequency by 2.

2. In step 4 how many times do you have to push PB2 before the flip-flop output toggles through an entire cycle (example: starts LO goes HI, then end LO) ?
   Answer: PB2 must be pushed twice.

5.3.5 Lab 5.5 Clocked D Flip-flops

5.3.5.1 Results

3. The truth table for this circuit is:

PB2	S1	L1
LHL	1	1
LHL	0	0

4. The flip-flop changes state on the positive going or leading edge of the clock pulse.

5.3.5.2 Questions and Answers

1. From the results of step 4 describe the switching action of the 74LS74.
   Answer: The 74LS74 is a positive edge triggered circuit.

2. Is this an active HI or active LO circuit ?
   Answer: The 74LS74 is an active HI logic circuit.

5.3.6 Lab 5.6 The J-K Flip-flop

5.3.6.1 Results

> NOTE
> The 74LS76 used in this lab uses pin 5 for Vcc and pin 13 for Ground.

3. The initial state of the latch is RESET.

4. The truth table for the J-K FF is:

S1	S2	PB2	L1	L2
0	0	LHL	Q	$\overline{Q}$
1	0	LHL	1	0
0	1	LHL	0	1
1	1	LHL	TOGGLE	

NOTE
Q indicates the previous or initial state of Q when the clock is pulsed.

6. In this configuration the J-K flip-flop acts as a toggle. This means the output frequency is one-half the input clock frequency.

8. The truth table for this circuit is:

S1	L1	L7
1	0	LHL
0	1	LHL

In this mode the J-K acts like a LO active D flip-flop.

5.3.6.2 Questions and Answers

5.11.4 Questions:

1. If both J and K inputs are held HI as in steps 5 and 6 what function is the J-K FF performing ?
Answer: This J-K configuration is a toggle.

2. What latch function does the circuit of step eight perform ?
Answer: This circuit is a D FF.

5.3.7 Lab 5.7

5.3.7.1 Results

3. L7 is stable LO.

4. The output on L7 was a short duration HI pulse.

6. The pulse in this step is shorter than the pulse obtained in step 4.

5.3.7.2 Questions and Answers

1. Name one use of a one-shot IC.
Answer: A one-shot is frequently used to debounce switch contacts.

2. Explain the name one-shot.
Answer: The device will give a single output pulse when a trigger is sensed on the input even if the trigger event occurs several times during the output pulse width, hence the name one-shot.

CHAPTER 6
DIGITAL ARITHMETIC

6.1 Objectives

Upon completion of this chapter the student should be able to:

- Understand binary addition with signed and unsigned numbers.
- Use the two's complement form of binary numbers to perform arithmetic.
- Multiply and divide binary numbers.
- Perform arithmetic operations on BCD and hexadecimal numbers.
- Implement digital arithmetic circuits.

6.2 Questions and Answers

1. What is the sum of 101 and 011 ?
   Answer: The sum is binary 1000.

2. Compute the difference between 011 and 010.
   Answer: The difference is binary 001.

3. What is meant by a half-adder ?
   Answer: A half-adder performs addition without a carry input from the next lower order bit. The half-adder has sum and carry outputs.

9. The truth table for the full adder is:

A	B	Cn	S	C
0	0	0	0	0
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1
0	0	1	1	0
0	1	1	0	1
1	0	1	0	1
1	1	1	1	1

A = S1, B = S2, Cn = S3, S = L1, C = L2

6.3.1.2 Questions and Answers

1. Explain the difference between a half-adder and a full adder.
Answer: The half-adder has no input for a carry from a lower order bit. Both types of adders have sum and carry outputs.

2. Use the truth table from step 9 to form the logic equations and Karnaugh maps for the full adder.
Answer:
The logic equation for the sum is:

$$S = ABCn + A\overline{B}\overline{C}n + \overline{A}B\overline{C}n + \overline{A}\overline{B}Cn$$

The logic equation for the carry is:

$$C = ABCn + AB\overline{C}n + A\overline{B}Cn + \overline{A}BCn$$

The K-map for the sum is:

	$\overline{A}\overline{B}$	$\overline{A}B$	AB	$A\overline{B}$
$\overline{C}n$		1		1
Cn	1		1	

The K-map for the carry is:

	$\overline{A}\overline{B}$	$\overline{A}B$	AB	$A\overline{B}$
$\overline{C}n$			1	
Cn		1	1	1

6.3.2 Lab 6.2 Parallel Binary Adder

6.3.2.1 Results

4. This circuit is connected so that the inputs act as unsigned magnitudes. The circuit adds 2 4-bit binary unsigned numbers and gives a 4-bit with carry output.

8. On initial power-up L0-L3 light and L4-L7 are off. L0-L3 display the one's complement of the number entered on S0-S3.

9. The circuit subtracts the number selected by S0-S3 from the

number selected by S4-S7. Positive results are shown with by carry assertion. Negative results are in a one's complement format. Two zeros exist. The "positive zero" occurs when the carry is set and L0-L3 are all LO. The "negative zero" occurs when the carry is clear and L0-L3 are all HI.

6.3.2.2 Questions and Answers

1. Describe the two different types of adders used in this laboratory.
Answer: The adder of step 4 adds two unsigned 4-bit numbers and gives a 4-bit with carry result. The second adder, step 9, subtracts the number applied to S0-S3 from the number entered on S4-S7 by adding the one's complement of S0-S3.

2. Show two ways that the 7483 can represent a 0 when connected as a one's complement subtractor.
Answer: The two zeros are shown below:

L0	L1	L2	L3	C	
0	0	0	0	1	positive
1	1	1	1	0	negative

3. What changes would have to be made for the circuit of step 8 in order for the circuit to add two positive binary numbers ?
Answer: Tie pins 2,5,9 and 13 to ground to disable the complement circuit and tie pin 13 to ground to disable the end-around carry.

6.3.3 Lab 6.3 The BCD Adder

6.3.3.1 Results

4. Sums of nine and below are displayed correctly. For sums between 10 and 15 inclusive, L7 lights while L0-L3 display the LSB. For sums between 16 and 20 inclusive, L6 lights while L0-L3 display the LSB. Sums greater than 20 give incorrect results. Non BCD inputs are not forbidden by this circuit and correct sums will be obtained within the limitations of the adder.

6. This circuit works similarly to the one in step four. The sum outputs now drive a seven segment display. The two carry outputs are combined by the 74LS27 to form a 1/2 digit output using the other seven segment display. The circuit is a BCD adder with a 1 1/2 digit decimal output. The device will add two BCD or hexadecimal numbers and display correct sums through 19.

6.3.3.2 Questions and Answers

1. What are the results when a number greater than 20 is the sum output for the circuit of step 6 ?
   Answer: The display is blanked.

2. What does the circuitry added to pins 1 and 2 of the 74LS27 in step 5 do ?
   Answer: This circuit uses the two carry outputs to form a 1/2 digit output which acts as the MSD of the sum.

NOTE
The data in this experiment are active LO.

6.3.4 Lab 6.4 The ALU

6.3.4.1 Results

3. The function performed by this circuit is F = A plus B. This is a binary adder with a 4-bit plus carry output.

6. The function performed here is A minus B minus 1. This is a one's complement subtractor without end around carry. Positive results are off by one. Negative results are correct.

8. The function here is F = A minus B. Now positive results are correct, negative results are off by one.

6.3.4.2 Questions and Answers

1. What sort of circuitry would be needed to perform an end around carry for the circuit of step 6 ?
   Answer: The carry output can be fed through an inverter to the carry input in order to perform the end around carry.

CHAPTER 7
COUNTERS AND REGISTERS

7.1 Objectives

Upon completion of this chapter the student should be able to:

- Understand the operation of ripple counters.
- Explain and understand MOD counters.
- Understand and implement UP/DOWN counters.
- Explain and understand registers and their applications.
- Build counter and register circuits.

7.2 Questions and Answers

1. Explain what is meant by a ripple counter.
   Answer: A ripple counter is formed from cascaded toggle flip-flops. The name comes from the way clock pulses, which are also the counter outputs, ripple through the counter stages when the count is changed.

2. What is the modulus of a counter ?
   Answer: The modulus or MOD of a counter is the number of steps the device can count.

3. What is the difference in the circuit connections for up and down counters ?
   Answer: For ripple counters, the complement output is used to drive the next counter stage instead of the true output.

Parallel counters use the complement as the output instead of the true output used for an up-counter.

4. Explain what is meant by a parallel or synchronous counter.
Answer: All flip-fops in the counter switch at the same time since the clock lines of the flip-flops are paralleled.

5. What is the advantage of a parallel counter over ripple counters ?
Answer: A parallel counter only requires one gate delay to change state. This results in a speed advantage for a parallel counter.

6. What is meant by a presettable counter ?
Answer: A presettable counter can be made to count from any number within it's range.

7. Why are counter decoder circuits used ?
Answer: To convert the counter binary output to a more useable form for display such as decimal or hexadecimal.

8. What is a strobe pulse and how is it different from a clock pulse ?
Answer: A strobe pulse is used to enable a counter decoder. The strobe is a slightly delayed clock signal that allows the counter to settle before the output isdecoded.

9. What is a shift register ?
Answer: A shift register is a linear array of flip-flops which can transfer data between adjacent elements.

10. How many different types of shift registers are there ? Name them.
Answer: The two types of shift register are shift-left and shift-right.

11. Give the names of the four different input/output configurations for shift registers.
Answer: The four shift registers I/O configurations are: serial-in/serial-out, serial-in/parallel-out, parallel-in/serial-out, and parallel-in/parallel-out.

12. What is a ring counter ?
Answer: A ring is formed by loading a one into a shift register element and connecting the register output to it's input. As the register is clocked, the one circulates through the elements of the shift register allowing a count equal to the number of register elements.

13. What are the advantages of ring counters over binary counters?
Answer: No decoding is required to determine the count of a ring counter.

14. What are the advantages of binary counters over ring counters?
Answer: Binary counters use fewer gates to implement a given count. For example, four flip-flops can implement a MOD 16 binary counter or a MOD four ring counter.

15. How many disallowed states are there for a 3 flip-flops ring counter ?
Answer: The number of disallowed states is 5.

16. What is a Johnson counter ?
Answer: A Johnson counter is a special type of ring counter formed by feeding the complement output of the shift register back to the register input.

17. How many disallowed states are there for a 4 flip-flop Johnson counter ?
Answer: The number of disallowed states is eight.

18. What is a universal shift register ?
Answer: A register capable of shifting either left or right and input or output data either serially or parallel.

7.3 Labs

7.3.1 Lab 7.1 UP/ DOWN Counters

NOTE
The 74LS76 has Vcc on pin 5 and ground on pin 13.

7.3.1.1 Results

4. The circuit is a MOD 4 binary up-counter with HI true outputs.

5. PB1 resets the counter.

9. The circuit is a MOD 4 binary down-counter with LO true outputs.

7.3.1.2 Questions and Answers

1. What is the modulus of each of the counters in this laboratory?
Answer: The modulus of both counters is 4.

2. How can the down counter be converted to display a HI true output ?
Answer: Use the complement flip-flop outputs to drive the clock input of the next stage and use the true flip-flop output to observe the count.

7.3.2 Lab 7.2 Synchronous Counters

7.3.2.1 Results

NOTE
The 74LS76 has Vcc on pin 5 and ground on pin 13.

3. The circuit is a synchronous MOD 4 up-counter.

7. The circuit is a synchronous MOD 4 down-counter with LO true outputs.

7.3.2.2 Questions and Answers

1. Fully describe both counter circuits in this laboratory.
Answer: The circuit of step 3 is a synchronous MOD 4 binary up-counter with HI true outputs. The circuit of step 7 is a synchronous MOD 4 binary down-counter with LO-true outputs.

7.3.3 Lab 7.3 IC Counters

7.3.3.1 Results

NOTE
The 74LS90 has Vcc on pin 5 and ground on pin 10.

4. The circuit is a MOD 10 up-counter or decade up-counter. Two types of decade counters, BCD and bi-quinary, can be implemented with the 74LS90. The counter implemented here is a BCD counter.

5. PB1 resets the counter.

9. This circuit is a MOD 16 up/down presettable binary counter with clear.

7.3.3.2 Questions and Answers

1. Will the counter count with the load input active ?

Answer: The counter will not count with the LOAD input active.

2. Can the counter be loaded with the clear input active ?
Answer: The counter cannot be loaded with the CLEAR input active.

3. What is the modulus of this counter ?
Answer: The modulus of the counter is 16.

4. How could you make a counter of modulus 7 using the 74193?
Answer: Connect the inputs of a three input AND gate to the counter outputs. Connect the AND gate output to the CLEAR line of the counter (pin 14). This implements a premature reset counter.

7.3.4 Lab 7.4 Shift Registers

7.3.4.1 Results

3. The circuit is a 3-bit shift right SISO shift register.

4. It takes 3 PB2 pulses to light L3. PB1 clears the register.

7. The circuit is an absolute load 3-bit PIPO shift register with clear.

7.3.4.2 Questions and Answers

1. Explain the operation of the gating circuits appearing between flip-flops in Figure 7-21.
Answer: The AND gates connected to PB1 are used to enable data loading from the switches, thus PB1 is normally LO and the outputs of these AND gates are normally LO unless data is being loaded. The AND gates connected to PB2 form the normal flip-flop connections for the shift register, thus PB2 is normally HI and the output of these AND gates is the output state of the adjacent flip-flop. The OR gates detect an active input and couple it into the data output of the flip-flop.

2. Do you have to reset the 74174 in step seven to load parallel data ?
Answer: No the circuit is an absolute load flip-flop.

3. Could you make a PIPO shift register using only the 74174 and the two OR gates? What would be the operational restrictions on such a circuit ?

Answer: Yes you could implement the PIPO using only OR gates. The operational restrictions are: The 74174 would have to be cleared before data was loaded, and all input data switches have to be set LO after data load and before the next clock cycle.

7.3.5 Lab 7.5 The 74165

7.3.5.1 Results

3. The circuit is a parallel load (by PB1) PISO shift register. When all bits are shifted out of the register, the display blanks since the serial input serves as the data source until load is activated.

4. A HI appears on the L0 output of the register on the eighth clock pulse. This HI is from the serial input.

7.3.5.2 Questions and Answers

1. How does the 74165 determine which input to receive it's data from. Describe how each data input is activated.
Answer: The 74165 will use the serial data input if the LOAD input is HI. When the LOAD input is LO data is loaded from the parallel inputs.

7.3.6 Lab 7.6 The 74164

7.3.6.1 Results

3. The circuit is a SIPO with clear and 8-bit output. S0 is the data input.

4. The circuit is the same as that of step three except that the data input is S1.

7.3.6.2 Questions and Answers

1. What happens if both S0 and S1 are LO ?
Answer: When both switches are LO, all inputs are LO.

2. How would you use this circuit as a SISO register ?
Answer: To use this IC as a SISO, observe the output on Qh the high order flip-flop output.

CHAPTER 8
INTEGRATED CIRCUIT LOGIC FAMILIES

8.1 Objectives

Upon completion of this chapter the student should be able to:

- Identify the two major IC logic gate families
- Use IC specification sheets
- Understand the use of tri-state logic circuits
- Interface the different logic families together in circuits
- Understand the need for Electrostatic Discharge (ESD) control

8.2 Questions and Answers

1. Name the two major types of logic devices.
   Answer: The two major types of logic devices are TTL and CMOS.

2. What are the logic levels for TTL circuits ?
   Answer: The logic levels for TTL are 0 VDC and 5 VDC.

3. Are propagation delays cumulative ?
   Answer: Yes propagation delays are cumulative.

4. Are rise times cumulative ?
   Answer: No rise times are not cumulative.

5. Explain the need for ESD protection around CMOS devices.
Answer: Electrostatic discharge can destroy a CMOS device by punching through the thin layer of silicon dioxide insulating the gate from the substrate material of the device.

6. Where are open-collector outputs used ?
Answer: Open collector outputs are most frequently used to implement wired logic. They are also used to implement logic circuits with output voltage and current levels that differ from standard TTL levels.

7. What are the states of a three-state device ?
Answer: The three states are: HI, LO and disconnected (high impedance).

8. What does MOSFET stand for ?
Answer: MOSFET is the acronym for Metal Oxide Semiconductor Field Effect Transistor.

8.3 Labs

8.3.1 Lab 8.1 TTL Loading Rules

8.3.1.1 Results

4. The output voltage should be about 5 VDC.

6. The output voltage should have dropped to about 4 VDC.

8. The output voltage should drop under 4 VDC.

8.3.1.2 Questions and Answers

1. What happens as the number of loads connected to a single TTL output increases?
Answer: The output HI voltage level will drop and the output LO voltage level will rise.

8.3.2 Lab 8.2 Open-Collector Logic Gates

8.3.2.1 Results

4. The inverter output remains LO for both input conditions.

5. The output "rises" a small amount but is far short of a TTL logic one.

7. The output, L1, displays the complement of the input.

11. The truth table is:

S1	S2	L1
0	0	1
0	1	0
1	0	0
1	1	0

8.3.2.2 Questions and Answers

1. What happens when an open-collector circuit does not have a pull-up resistor?
   Answer: The circuit output will be unable to reach a TTL high since it has no connection to Vcc.

2. What logic function is performed by the circuit in step 11?
   Answer: The circuit is a two-input wired NOR gate.

8.3.3 Lab 8.3 Three-State Logic

8.3.3.1 Results

4. With S2 HI and S1 LO, the output appears disconnected.

5. With S2 HI the device is disconnected at it's output. When S2 is LO, L1 = S1.

8.3.3.2 Questions and Answers

1. What is the function of the control input?
   Answer: The control input is used to enable the gate output.

2. Is this a true or inverting bus driver?
   Answer: This is a true (non-inverting) bus driver.

3. What is another name for bus driver?
   Answer: Another name for bus driver is buffer.

8.3.4 Lab 8.4 TTL and CMOS Interfacing

8.3.4.1 Results

4. The truth table is:

S1	S2	L1
0	0	0
0	1	0
1	0	0
1	1	1

6. The truth table is:

S1	S2	L1
0	0	0

S1	S2	L1
0	1	0
1	0	0
1	1	1

8.3.4.2 Questions and Answers

1. What is the function of the resistors in steps 3 and 5?
   Answer: The resistor in step 3 is a pull-down resistor while the resistor in step 5 is a pull-up resistor. They are used to shift logic levels.

2. Name two advantages of CMOS logic.
   Answer: Some advantages of CMOS logic are: low power consumption, high noise immunity, high fan out, and a wide range of useable supply voltages.

CHAPTER 9
MEDIUM SCALE INTEGRATION

9.1 Objectives

Upon completion of this chapter the student should be able to:

- Explain and define MSI circuits
- Name several common types of MSI circuits
- Know when to use MSI circuits vs. other types of logic circuits.

9.2 Questions and Answers

1. Define MSI circuit.
   Answer: An MSI circuit is a device which integrates 12 to 100 transistors onto a single piece of silicon.

2. What alternatives are available for the implementation of logic circuits ?
   Answer: Logic circuits of medium complexity are easily implemented with MSI logic, Read Only Memory, and programmable logic arrays.

3. What is the basic decoder circuit ?
   Answer: The basic decoder circuit is the AND gate.

4. Name the basic encoder circuit.
   Answer: The basic encoder circuit is the NAND gate.

5. Define a digital multiplexer.
   Answer: A digital multiplexer routes one of several digital

inputs to a single output.

6. Describe a digital demultiplexer.
Answer: A digital demultiplexer routes a single input to one of several outputs.

7. Give two applications of decoders.
Answer: Two typical decoder applications are the BCD/decimal decoder and the BCD/7-segment decoder.

8. What are three applications of multiplexers ?
Answer: Three applications of multiplexers are: data selection, parallel to serial conversion, and Boolean function generator.

9. Name an application of demultiplexers.
Answer: Data distribution and serial to parallel conversion are two common demultiplexer applications.

10. How many control lines are needed for a 16 input multiplexer?
Answer: A 16 input multiplexer requires 4 control lines.

9.3 Labs

9.3.1 Lab 9.1

9.3.1.1 Result

3. The circuit is a four-line to 10-line or BCD/DEC decoder.

9.3.1.2 Questions and Answers

1. What happens to the outputs when a count greater than nine is entered onto the binary input lines ?
Answer: All outputs are high for invalid data.

2. What type of circuit could you use to tell that an invalid input had been entered on the S0-S3 inputs ?
Answer: A ten input and gate connected to the decoder outputs would indicate invalid input conditions.

3. What type of circuit would you need to use to detect invalid inputs for the 3-line to 8-line decoder ?
Answer: A simple two-input AND gate with inputs from Vcc and S3 will indicate invalid input data for the 3-line to 8-line decoder.

4. Are the outputs of the 74LS42 LO true or HI true ?
Answer: They are LO true.

5. The LD-2 has an internal display driver so that the outputs of the 74LS42 are driving a TTL load and not a directly connected LED. Can the 74LS42 be used to drive an LED indicator directly? Explain your answer.
Answer: The low level output current, 8 mA., means the 74LS42 is poorly suited to driving LEDs which require about 20 mA. for good brightness.

9.3.2 Lab 9.2 Decoder/Drivers

9.3.2.1 Results

2. The basing diagram for the TIL 312 is:

Pin	Segment
1	a
2	f
7	e
8	d
10	c
11	g
13	b

4. The circuit is a BCD/7-SEG decoder/driver. The LD-2 uses a CD4511 as a display driver instead of the 7447.

9.3.2.2 Questions and Answers

1. Is the display clear ? How could this be improved ?
Answer: The display is not clear. A red filter, like the one on the LD-2, would help considerably.

2. What is the purpose of the 330 ohm resistors ?
Answer: The 330 ohm resistor serves as a pull-up for the open-collector output of the 7447, and limits the current through the display segments.

3. What count is displayed when the TIL 312 consumes the greatest power ?
Answer: The maximum power is consumed when the count is 8.

4. What input is required to blank the display ?
Answer: An input of 1111 binary will blank the display.

9.3.3 Lab 9.3

9.3.3.1 Results

4. The circuit is an eight-line to three-line priority encoder with LO active inputs and outputs. A priority encoder will only encode the input with the greatest weight when more than one input is active. The GS output is HI only when the inputs are all HI.

9.3.3.2 Questions and Answers

1. Are the inputs to the 74LS148 LO true or HI true ?
   Answer: The inputs are LO true.

2. Are the outputs used in this experiment LO true or HI true?
   Answer: The outputs are also LO true.

3. Explain what is meant by a priority encoder ?
   Answer: When more than one input is active the priority encoder only encodes the highest order input.

4. How can you tell the difference between a zero input and no input ?
   Answer: The GS output will be LO for a zero input.

9.3.4 Lab 9.4

9.3.4.1 Results

4. The circuit is a 4-input multiplexer.

6. The truth table is:

S6	S7	L7
0	0	0
0	1	0
1	0	0
1	1	1

9.3.4.2 Questions and Answers

1. Explain the operation of the 4-line to 1-line multiplexer.
   Answer: The A and B control inputs (S6 and S7) select which data input of C0-C3 (switches S0-S3) is routed to the output (L7).

2. How would you implement the logical EXNOR using a 74LS153 ?
   Answer: Use the circuit from the lab with inputs C0 and C3 HI and inputs C1 and C2 LO.

9.3.5 Lab 9.5

9.3.5.1 Results

3. The circuit is an eight output demultiplexer. The data on S7 is routed to the output selected by S0-S2. The outputs which are not selected remain HI.

9.3.5.2 Questions and Answers

1. Since the demultiplexer is the inverse function of the multiplexer, could the 74LS138 be used for serial to parallel conversion ?
   Answer: The 74LS138 can be used for serial to parallel conversion.

2. What type of circuit is a demultiplexer made from ?
   Answer: Any decoder with one or more enable inputs can be used as a demultiplexer.

CHAPTER 10
DATA CONVERSION/ ACQUISITION

10.1 Objectives

Upon completion of this chapter the student should be able to:

- Explain the basic operation of a digital to analog converter.
- Understand the operation of an analog to digital converter.
- Name two types of analog to digital converters.
- Understand basic sample; and hold circuits.

10.2 Questions and Answers

1. Name the three general areas of DAC specification that are the most important in determining device performance.
   Answer: The three most important areas of DAC specification are resolution, accuracy, and speed.

2. Name two types of ladder circuits used in DACs.
   Answer: Two types of DAC ladder circuits are the binary R-2R and the simple voltage divider network where $Rn = Ro/2^n$.

3. Give two applications for DACs.
   Answer: They are used to convert data to analog signals and in A/D converters.

4. Name two types of A/D converters.
   Answer: Two types of A/D converters are the simultaneous or flash converter and the sequential or serial converter.

5. What parts are required to form a successive approximation A/D ?
Answer: The elements of a successive approximation A/D are the control logic, a successive approximation register, a comparator, a DAC and an output latch.

6. What is data acquisition ?
Answer: A process where analog data is converted to binary data and stored.

7. What part of a sample and hold circuit performs the hold function ?
Answer: The capacitor holds the voltage.

8. Give two reasons for using sample and hold circuits in data acquisition.
Answer: These circuits improve the stability of the A/D conversion process for rapidly changing signals and hold the data on systems with multiplexed analog inputs.

9. Explain the difference between analog and digital multiplexers.
Answer: Digital multiplexers have binary outputs and can be constructed from logic gates. Analog multiplexers can have a wide range of output voltages and are electrically equivalent to a rotary switch.

10.3 Labs

10.3.1 Lab 10.1 D/A Converters

10.3.1.1 Results

5. The circuit is an eight-bit D/A converter. The output is Vo = 10 V (A1/2 + A2/4 + ... A8/256). The resolution of the converter is 0.39% or 39 mV.

10.3.1.2 Questions and Answers

1. What is the theoretical resolution of this D/A converter ? Did your circuit exhibit this resolution.
Answer: The theoretical resolution is 0.39%. This should have been the observed resolution.

2. What is the purpose of the op-amp in the circuit of Figure 10-10 ?
Answer: This op-amp converters the current output of the

DAC to voltage.

3. What is the maximum output of the A/D converter ?
Answer: The maximum output is 100% or 10 volts in this lab.

4. What type of output does the D/A provide ? Could you use this output directly or would you need some filtering to make this a useable output ?
Answer: The output changes in discrete steps. Some low-pass filtering is needed to make the output signal more useable.

10.3.2 Lab 10.2 A/D Converters

10.3.2.1 Results

5. This circuit is an A/D converter which outputs a eight-bit integer proportional to a 0-5 V analog input. Output = binary equivalent of (Vin/5 V)255

10.3.2.2 Questions and Answers

1. What is the theoretical resolution of this type of converter ? How does this compare with the value that you measured ?
Answer: The resolution of this converter is 0.39% or about 19 mV for the lab circuit.

2. What is the maximum frequency of the analog signal that the laboratory circuit can convert ?
Answer: The maximum frequency input for this converter is about 780 Hz.

3. How many clock cycles are required for the ADC 0809 to complete a conversion ?
Answer: The ADC 0809 needs 64 clock cycles to complete a conversion.

10.3.3 Lab 10.3 The Analog Multiplexer

10.3.3.1 Results

4. The circuit is an analog multiplexer connected to an A/D converter. The output of the multiplexer will be (n/7)5 V where n is the number selected on S0-S2. The display output will be the binary equivalent of (n/7)255.

10.3.3.2 Questions and Answers

1. Explain the difference between an analog multiplexer and a digital multiplexer ?
Answer: A digital multiplexer can have only two output

states while an analog multiplexer can have a wide range of output voltages.

2. How much does the count change on L0-L7 when the input on A-C is changed by one.
   Answer: The count should change by about 36 for a change in input of 1.

CHAPTER 11
POTPOURRI

11.1 Objectives

Upon completion of this chapter the student should be able to:

- Identify the uses of the 555 IC.
- Describe an opto-isolator and it's uses.
- Understand the need for and application of DIP relays.
- Define ROM and explain some typical ROM applications.
- Understand what programmable logic devices are and name the leading types of programmable logic devices.

11.2 Questions and Answers

1. Is the 555 timer a digital or analog circuit ?
   Answer: The 555 timer provides a digital output but most of it's internal circuitry is analog so it is frequently classified as an analog device.

2. When would an opto-isolator be useful ?
   Answer: An opto-isolator is used to allow circuits to transfer signals while remaining electrically isolated.

3. Name some uses of a DIP relay.
   Answer: A DIP relay can be used to control high voltage or current loads with TTL level signals. DIP relays are available

in almost any imaginable contact arrangement and are common in switching circuits.

4. Name three types of programmable logic devices.
Answer: Three types of programmable logic devices are PALs, ROMs, and PLAs.

5. Explain the difference between PALs, PLAs and ROMs.
Answer: The PAL has a programmable AND gate array and a fixed OR gate array on the output. The ROM has a fixed AND gate array which decodes the input fully and a programmable OR gate array for the output. The PLA has programmable AND gate input and OR gate output arrays.

11.3 Labs

11.3.1 Lab 11.1 The 555 Timer

11.3.1.1 Results

4. The circuit is a one-shot. It provides a single output pulse of fixed width. The circuit will not accept additional inputs until the output returns to LO.

11.3.1.2 Questions and Answers

1. Is the circuit of Figure 11.5 retriggerable ?
Answer: No this circuit is not retriggerable.

2. Name one use of the astable circuit ?
Answer: This circuit can be used as inexpensive oscillator to drive a speaker or other device.

3. Can a 555 produce a 50% duty cycle output ?
Answer: The basic astable circuit cannot produce a 50 % duty cycle output. This occurs because if Ra = 0 the discharge current for the capacitor in the 555 will exceed the current rating of the discharge transistor.

4. Is a 555 a digital circuit ?
Answer: While the output is digital the 555 is an analog circuit.

11.3.2 Lab 11.2 DIP Relays

11.3.2.1 Results

2. When S0 = HI, relay contacts are open. S0 = LO, relay contacts are closed and L7 is lit.

3. The current reading should be about 0.110 A.

11.3.2.2 Questions and Answers

1. Could you use a normal TTL circuit to drive the relay ? Why?'
Answer: A normal TTL circuit cannot be used to drive this relay since the current requirements of the relay coil are beyond the capability of TTL circuits.

2. Name one application of relays.
Answer: Relays are used to switch high voltage or current signals at the relay contacts with a small voltage applied to the relay coil.

3. If a normal TTL device cannot drive a relay directly then what is the advantage of having a 5 V relay coil ?
Answer: The 5 V relay coil still allows control of the relay by a TTL device connected to a switching transistor.

11.3.3 Lab 11.3 The Opto-Isolator

11.3.3.1 Results

2.

S0	L0
H	H
L	L

3. When S0 = ON, Vout = 12 V. When S0 = OFF, Vout = 0 V.

11.3.3.2 Questions and Answers

1. Name three types of light sources.
Answer: Three types of light sources are LEDs, tungsten lamps and neon lamps.

2. Name two types of light detectors.
Answer: Common detectors are phototransistors, photodiodes, photoresistors, and light activated SCRs and TRIACs.

3. Define opto-isolator.
Answer: An opto-isolator is a device containing a light source/sensor pair.

4. Does the circuit of Figure 11-8 invert the input signal ?
Answer: This circuit is non-inverting.

5. Does the circuit of Figure 11-8 convert from TTL to CMOS ?
Answer: The circuit will convert from TTL to CMOS levels.

11.3.4 Lab 11.4 Implementing Logic Functions with ROMs

11.3.4.1 Results

5. The addresses and outputs in hexadecimal are:

Address	Output
000	30
001	31
002	32
003	33
004	34
005	35
006	36
007	37
008	38
009	39
00A	41
00B	42
00C	43
00D	44
00E	45
00F	46

11.3.4.2 Questions and Answers

1. How many memory locations does the 2864 have ?
   Answer: The 2864 has 8192 8-bit memory locations.

2. How many bits can each location store ?
   Answer: Each location is 8-bits wide.

3. Would you normally use this ROM for this application ?
   Answer: No, this ROM is far more complex than the one needed to implement this circuit since only 16 of 8192 memory locations were used.

CHAPTER 12
MICROCOMPUTER CONCEPTS

12.1 Objectives

Upon completion of this chapter the student should be able to:

- Define microcomputer in relation to mainframes and minicomputers.
- Understand the basic organization of a microcomputer.
- Explain how computers are programmed.
- Understand the basics of microcomputer interfacing.

12.2 Questions and Answers

1. Give an example of a situation where a mainframe computer is used?
   Answer: A mainframe is used by the IRS to keep tax payer records. A mainframe is used because of its high speed and large amount of storage.

2. Give an example of a situation where a microcomputer is used. Why?
   Answer: A microcomputer is used in many popular arcade games. The microcomputer is chosen for its high cost/performance ratio and the ease with which a custom system, such as an arcade game, cab be packaged compactly.

3. Why isn't the address bus in a computer bi-directional?
   Answer: The address bus is used by the processor to select

memory or I/O devices. The memory and I/O devices do not select the processor so there is no need for the address bus to be bi-directional.

4. What is micro code ?
   Answer: Micro code is the program inside the microprocessor which is continually running allowing the microprocessor to read and execute commands from external memory.

5. Why is digital logic used in modern computers ?
   Answer: Digital logic is used in modern computers since it is easily implemented with common 2-state switching circuits.

6. What is the primary difference between RAM and ROM?
   Answer: Data stored in RAM is lost when power is removed from the computer system while data in ROM is retained.

7. If a serial communications port can transmit at a rate of eight bits/second, what is the equivalent parallel port transmission speed ?
   Answer: The equivalent speed for and eight bit parallel port is one byte/sec or transfer per second.

8. How is object code obtained from an assembly language program?
   Answer: A special program called an assembler converts the assembly language mnemonics to object code.

9. Why are three bytes required for a typical machine code jump instruction ? Label the three bytes that make up the typical machine code "jump" instruction (i.e. data, instruction, address)
   Answer: The first byte is the jump instruction. The next two bytes are the low and high order address bytes that tell the microprocessor where to jump.